A Double-Gain, Large Dynamic Range Front-end ASIC With A/D Conversion for Silicon Detectors Read-Out

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Abstract—We present a prototype of an application specific integrated circuit (ASIC) featuring an input dynamic range of more than 52 pC. The ASIC is designed to read out signals from large-capacitance silicon detectors used in Si-W calorimeters for high-energy astroparticle physics experiments. The ASIC features a double-gain Charge Sensitive Amplifier (CSA), which uses a real-time automatic gain selection circuitry to switch between the input ranges of [0–2.4 pC] and [0–52.6 pC]. A Correlated Double Sampling (CDS) filter follows the CSA and completes the front-end chain. A complete analog channel dissipates 2.8 mW. The present prototype also includes 9 cyclic ADC channels, in view of the final objective of this project, which will be a 16-channel chip with digitized outputs.

Index Terms—Astroparticle experiments, double-gain preamplifier, front-end electronics, Si-W calorimeters.

I. INTRODUCTION AND MOTIVATION

FOR many years the exploration of the “knee” region (i.e., at an energy around \(10^{15}–10^{16}\) eV) of the Cosmic-Ray spectrum has been carried out by means of very large area experiments on Earth. These experiments measure the secondary particles produced by the interaction of the very-high energy cosmic particles with the atmosphere (see, e.g., [1]). Recently, several satellite-borne experiments have been proposed to perform direct measurements of the primary fluxes at and above the TeV region using different approaches [2]–[4]. Silicon-tungsten (Si-W) calorimeters represent an excellent solution for balloon- or satellite-borne experiments, given their very good dE/dx measurement capability, efficiency, linearity, compactness and low-voltage operation. An example of the maturity of this technology and of its current capabilities is given by the Si-W electromagnetic imaging calorimeter of the satellite-borne experiment PAMELA [5], [6].

However, in view of the above mentioned high energy experiments, one of the most delicate issues encountered is the lack of a suitable front-end electronics required to read the very large signals that develop in the calorimeter as a result of the electromagnetic and hadronic interactions of such high-energy particles [2], [3]. In the framework of the INFN R&D projects CASIS and CASIS2, we are developing several application specific integrated circuit (ASIC) prototypes to address this problem.

The first prototype, CASIS1.0, was designed and tested in 2005–2006 [7]. In this paper, we report on the design and performance of the second prototype of the chip (CASIS1.1), which has been designed and fabricated in a CMOS 0.35 \(\mu\)m technology (AMS C35B4C3 with 4 metal and 2 polysilicon layers, supplied with a single voltage of 3.3 V). The prototype features 2 complete front-end channels and 9 fully differential cyclic (algorithmic) ADC channels, based on two different design approaches for the differential opamps.

The design goals for the front-end part were to achieve a dynamic range of 50 pC (\(\sim 10^{4}\) Minimum Ionizing Particle, or MIP, for 380 \(\mu\)m thick silicon sensors), a signal-to-noise ratio of at least 5:1 for 1-MIP signals with a detector capacitance of 300 pF, a linearity better than 1% over the full range, and to limit the power consumption to less than 3 mW/channel.

For the ADC, the design goals were to achieve a conversion time of less than 15 \(\mu\)s, a resolution of 12 bit and a power consumption comparable with that of the front-end section.

The final objective of the project is to pertain to a 16-channel ASIC in two versions. The first version will feature a more “conventional” architecture, with 16 preamplifier-shaper channels, followed by an output multiplexer to serialize the analog signals onto a single output bus. The second version will implement also the A/D conversion function, by integrating one ADC/channel.

The design architecture of the circuit and the CMOS implementation are described in Section II. Experimental results are presented in Section III, while conclusions and future developments are discussed in Section IV.

II. DESIGN ARCHITECTURE AND CMOS IMPLEMENTATION

A. Front-end Section

Fig. 1 presents a schematic block diagram of the front-end section of the ASIC. To allow for the very large design dynamic range, we have developed a new Charge Sensitive Amplifier (CSA) architecture based on a double-gain loop with an automatic gain-selection circuitry: a 1.6 pF feedback capacitor is permanently connected to a folded cascode amplifier, thus defining the high gain. A real-time feedback control network senses the CSA output and automatically inserts a second, large (30.4 pF) capacitor in the feedback loop (thus setting...
the low gain) when the input signal exceeds a threshold set at \(500 \text{ MIP}\).

The CSA is designed around a classical folded cascode block whose input PMOS transistor has been dimensioned to cope with the very large expected detector capacitance (\(350 \text{ pF}\)). The voltage swing at the CSA output is 1.5 V and the nominal sensitivities for high- and low-gain are 3 mV/MIP and 0.15 mV/MIP, respectively. The CSA output is sampled by a Correlated Double Sampling (CDS) filter. The system is reset periodically (Fig. 1). The minimum CSA reset width in order to completely discharge the feedback capacitors in the worst case has been verified to be 160 ns. On the other hand, the CDS reset duration has to take into account the settling time of the CSA, which is 400 ns with a detector capacitance of 300 pF. When a trigger is present, a HOLD signal is generated after a fixed (adjustable) delay \(t\) from the last reset pulse, and at the output of the CDS operational amplifier appears the difference between the baseline and the signal. The choice of the CDS time constant \(t\) depends on the particular application, and is a trade-off between the need to reduce the dead time of the system while keeping the parallel noise contribution to an acceptable level. As an example, the parallel noise due to a detector leakage current of 100 nA (a rather high value) integrated in 10 \(\mu\text{s}\) is about 2500 e\(^{-}\)MIP. A “GAIN HOLD” signal is used to “freeze” the GAIN status after the output of the CSA has settled, in order to avoid possible noise-induced gain changes shortly before the HOLD time for signals very close to the threshold. The DC pedestal of the CDS output (normally set at 900 mV) can be externally adjusted by means of the \(V_{\text{pe}}\) bias.

A gate diagram of the real-time feedback control network is given in Fig. 2. To minimize power consumption and guarantee a fast response, the comparator of the feedback control network is implemented by a Schmitt trigger, with a hysteresis of a few hundreds mV. The Schmitt trigger’s output is connected to a SR-type flip-flop to avoid oscillations when the high gain is selected. The threshold of the Schmitt trigger is set at a voltage corresponding to an input charge of \(500 \text{ MIP}\). Notice that the threshold value does not need to be known \textit{a priori} with very high precision, since the charge integrated on the 1.6 pF capacitor in Fig. 1 is not destroyed when the system switches to low gain, thus enabling a precise calibration of the range. The feedback control network provides a “GAIN” output that gives the CSA gain status for each event (GAIN = “0” \(\rightarrow\) high gain, GAIN = “1” \(\rightarrow\) low gain). For test purposes, the G2SEL input can be used to select the range to be calibrated.

### B. ADC Section

As mentioned in Section I, one of the final versions of the ASIC will include one ADC/channel. This solution will avoid driving low-level analog signals (which are obviously very sensitive to pick-up noise) from the output of the front-end ASIC to an external ADC. Moreover, it will allow a greater compactness of the read-out chain, which is an important advantage in every experimental situation where there are constraints to the available physical space (such as, e.g., for satellite-borne detectors).

Because of its low power consumption, good overall performance and small silicon area, we selected a cyclic (algorithmic) ADC architecture [8]. The ADC has been designed for 12-bit resolution and a maximum clock frequency of 10 MHz. It should be noticed that a resolution of 12 bit is required in order not to degrade the signal-to-noise ratio for 1-MIP signals (a 3 mV signal of 1 MIP would correspond to 8 ADC counts). The design is based on a switched-capacitor, fully differential approach that allows good clock feed-through and charge injection immunity.
Fig. 3 shows a schematic block diagram of the ADC. The analog core of the circuit consists of two differential opamps: the first stage implements the twofold function of single-ended to differential conversion for the CDS output and of sample-and-hold circuit for the successive conversion steps. The output of the first differential opamp is compared by a clocked comparator, whose output is used to subtract or add a reference voltage at the input of the second differential opamp if the input signal is positive or negative, respectively. The resulting voltage is amplified by 2 and fed back to the input of the first amplifier, which now acts as a sample-and-hold circuit, and the cycle is repeated for the required number of clock pulses (corresponding to the desired bit resolution).

1) Differential Opamp Design: The achievement of a precise gain of 2 for the multiplication of the remainder is the most critical point in any type of cyclic ADC. The most important nonidealities that affect the gain of the multiply-by-2 function are mismatches in the capacitors defining the closed-loop gain, charge injection through the CMOS switches and finite amplifier open-loop gain.

The effect of the capacitor mismatch will be discussed later in Section III, while the charge injection effects (which results in gain and nonlinearities errors) are reduced by the fully differential architecture and by properly sequencing the operation of the switches, i.e., first opening switches at common mode potential at the end of each phase [9], [10].

On the other hand, the open-loop amplifier gain $A_{OL}$ must be high enough to cope with the desired resolution. For 12-b accuracy, this implies that $A_{OL} \geq 84$-dB.

The architecture of the first prototype, CASIS1.0, featured five complete front-end channels (based on the same design described in the previous subsection), each followed by a fully-differential cyclic ADC.

The results of the measurements performed on the CASIS1.0 chip had shown that the front-end section (CSA + CDS) fulfilled all design specifications, while the ADC channels displayed lower accuracy and larger power consumption with respect to the specifications, as well as a low yield (the percentage of working ADC channels was $\sim 50\%$) [7], [11]. The origin of the problem was identified in the effects of the random device mismatch in the input differential cascode amplifier of the differential opamps (Fig. 4(a)). In ideal conditions, the outputs $V_{dh}$ and $V_{db}$ of the differential stage are balanced around the bias potential $V_{BIAS}$ and therefore the output buffer is properly biased. In a real situation, however, random device mismatches can unbalance the mean value of $V_{dh}$ and $V_{db}$, thus generating an under- or over-bias of the output buffer. As a result, the common-mode feedback circuit cannot compensate for the imbalance and the circuit ceases to function. To solve this problem, we have revised the differential opamp design in CASIS1.1 by adding an additional common mode feedback circuit (shown in Fig. 4(b) to the input differential amplifier, and resizing the current mirror.
transistor. We designed two sub-types of this basic differential opamp, called N (for “Normal”) and F (for “Fast”). The sub-type F has been optimized for speed (at the expense of power consumption) by reducing the length of the transistors in the active load of the input differential amplifier and in the output buffer (see Table I).

An alternative design solution (considered as a back-up in case the basic design should have displayed some unexpected problem) was studied for the differential amplifier of the ADC.

It is based on a single-stage (inherently more tolerant to random device mismatch than a two-stage amplifier) folded cascode operational transconductance amplifier (OTA) with “gain enhancement” (Fig. 5). The gain enhancement technique [12] was used because it was not possible otherwise to achieve the high open-loop gain necessary for 12-b resolution with a single-stage amplifier. The gain-enhanced differential OTA design has been labelled Type O (for “OTA”). The Type O has the advantage over the other two types of a lower power consumption, and the disadvantages of a reduced speed and a larger silicon area (about 20% more than Types N and F).

Table I summarizes the main properties of the various amplifier designs.

2) Comparator Design: The comparator is based on the Output Offset Storage architecture proposed in [13] (see Figs. 10–12 in that Reference). During the inactive clock phase, the comparator inputs are connected to the common-mode voltage $V_{CM} = VDD/2$ and the offset of the differential amplifiers is stored on capacitors, so that it can be removed during the “comparison” phase. Monte Carlo simulations of the circuit (including both device process variations and random device mismatch) showed a standard deviation value of the offset distribution of $\sim 140 \mu N$. 

![Fig. 4. (a) Schematic diagram of the differential opamp implemented in the ADC of the chip CASIS1.0. (b) Revised input differential amplifier circuit as implemented in 6 ADC channels of CASIS1.1. The differential pair added in the new design to counteract the effect of random device mismatches on $V_{in}$ and $V_{out}$ is drawn with dashed lines.](image1)

![Fig. 5. Schematic of the folded-cascode OTA used as alternative design for the differential opamp of the ADC. The OTAN and OTAP amplifiers are used to enhance the DC-gain of the single stage OTA by increasing the output resistance of the cascode stack.](image2)

![Table I: Simulated characteristics of the amplifiers](table1)
C. CMOS Implementation

The prototype has been designed in the 0.35 μm C35B4C3 CMOS technology from Austriamicrosystem [14], which features four metal and two polysilicon layers. The supply voltage is 3.3 V.

In the design of the layout, special care has been taken to avoid coupling between the front-end section and the ADC. Separate power supplies and guard-rings have been used for the CSA, for the CDS and the analog circuits of the ADC and for the digital circuits (including the comparator).

Fig. 6 is a photograph of a chip. The dimensions are 3.1 mm × 3.1 mm. In this chip we realized two complete front-end channels (with an output buffer after the CDS), and nine ADC channels with different opamp designs: six are based on the basic telescopic differential opamp design of Fig. 4 (three Type N, “normal”, and three Type F, “fast”, see previous subsection) and three are based on the gain-enhanced OTA of Fig. 5.

III. EXPERIMENTAL RESULTS

A printed circuit board has been designed and realized to accommodate the chip under test (encapsulated in a CQFP64 package) into a socket, and to provide all necessary supply and bias voltages and currents. Fig. 7 shows a simplified block scheme of the test set-up. Charge could be injected into any (or both) of the two front-end channels by means of a pulse generator and a set of calibrated test capacitors. Another set of calibrated capacitors could be shunted at the preamplifier’s input to simulate various detector capacitive loads. A second control/data acquisition board (based on an FPGA) generated all control and logic signals for both the front-end and the ADC parts of the chip. The range, linearity and noise measurements on the front-end channels were performed with a 16-bit external ADC, while a 16-bit DAC was used to characterize the ADC response. In addition, the outputs of the two analog channels could be connected to the input of any ADC, thus enabling the test of the entire chain.

A. Front-end

The measurements presented in this subsection were performed using a CDS time constant $t = 10$ μs and a time duration of the reset signals for the CSA and CDS of 160 ns and 560 ns, respectively. Fig. 8(a) shows the response of the front-end circuit to four different input charge signals corresponding to 100, 200, 300 and 400 MIP, respectively. The transition from high gain to low gain is exemplified in Fig. 8(b), which displays a signal corresponding to about 500 MIP (slightly below threshold) and a signal slightly above the gain change threshold. Fig. 8(c) shows the circuit response (in low gain mode) for four input signals of 8000, 9000, 10000 and 11000 MIP. We would like to underline that the slow rise of the signal after a few hundreds of ns is due to the fact that the pulse generator output exhibited a long and slow “tail” component after the programmed voltage step. As stated in Section II-A, the real CSA settling time is 400 ns (at a level of 1%) with a detector input capacitance of 300 pF.

The measured dynamic range of the front-end circuit is 560 MIP in high-gain mode and more than 11000 MIP (or about 52.6 pC) in low-range mode (Fig. 9). The sensitivities are, respectively, 2.94 mV/MIP and 146 μV/MIP. Fig. 10 shows the measured non-linearity, expressed as the deviation of each measured point from the linear fit, for both gains. The maximum non-linearity is < 0.3% for high gain and < 0.6% for low gain.

The noise performance of the front-end section is displayed in Fig. 11. The measured equivalent noise charge (ENC) at zero input capacitance is 2278 e−rms, with a noise slope of ~7.5 e−/pF. The measured power consumption of the front-end section is 2.8 mW/channel.

Fig. 12(a) shows the result of a measurement performed by connecting the output of the CDS of one channel to all the ADC channels of the same chip. The purpose of this test was to verify the functioning of the entire chain. The test was done by injecting into the CSA a series of signal charges from ~10 to ~500 MIP. All nine ADCs respond correctly to the signal levels from the CDS shaper. Fig. 12(b) shows the corresponding integral non linearity (INL) of the entire chain for all the ADCs. The overall maximum non-linearity is about 18 ADC units, or ~0.4%. Although measured for only a few points, this result is fully compatible with the non-linearity of the front-end (Fig. 10).
B. ADC

The first test that was performed on the ADCs was a fast functionality and power consumption measurement aimed at ensuring that the random device mismatch problems had been solved. The results of this test have shown that all 171 ADC channels of the 19 prototypes tested function normally (i.e., convert correctly) and display a normal power consumption (that is \(\sim 3 \text{ mW for Type O}, ~\sim 4 \text{ mW for Type N and } \sim 8.6 \text{ mW for Type F}\)). These results clearly indicate that both versions of the ADC are immune to the device mismatch effects that affected the previous version.

The characteristics of the ADCs were studied by means of an external 16-bit DAC. The input voltage level was varied in steps of 400 \(\mu\text{V}\). Fig. 13 shows the transfer curve of one Type N ADC, operated at a clock frequency of 1 MHz, over its full range of 1.7 V. For 12-bit resolution, the theoretical value of a single bit is 415 \(\mu\text{V}\). From a linear fit of the response, we obtain a 1-bit value of 420 \(\mu\text{V}\), very close to the design value. From this measurement we can observe that the open loop gain of the differential opamps is compatible with the design sensitivity of 12 bit.

The ADC linearity, on the other hand, is not yet satisfactory. This is essentially due to a known drawback of conventional restoring cyclic ADCs, namely the loop gain error (due to mismatches in the capacitor values used to implement the multiplication by 2) [10]. The effect of this error on the transfer characteristic of the ADC is clearly visible in Fig. 14, which displays a magnification of the central region (i.e., for input signals very close to the common mode voltage \(V_{\text{CM}}\)) of Fig. 13.

The INL of the ADC over the entire 1.7 V input range is shown in Fig. 15. The measurement clearly shows that the INL is not symmetric with respect to the middle of the range. This is due to a non linearity in the single-ended to differential conversion originating from the fact that the input common mode variation with the input signal exceeds the linear range.

From Fig. 15 it is also evident, again, the effect of the gain error, while no appreciable offset error appears, thus confirming the expected comparator offset performance. The measured INL...
Fig. 10. Measured non-linearity of the front-end chain for high-gain (a) and low-gain (b) modes.

Fig. 11. Measured equivalent noise charge of the front-end chain as a function of the input load capacitance.

Fig. 12. Response of all ADCs of one chip fed by the CDS output of a front-end channel (a), and corresponding INL of the entire (front-end+ADC) chain (b).

Fig. 13. Measured transfer characteristics of an ADC channel over the full input range (1.7 V).

corresponds to an effective resolution of 9.2 bit in the lower half range and of 8.4 bit in the upper half-range.

IV. SUMMARY AND FUTURE WORK

The second prototype (CASIS1.1) of a VLSI front-end chip intended for the read-out of silicon calorimeters in future high-energy astroparticle physics experiments has been designed, produced and tested in the framework of the INFN R&D project CASIS2. The prototype features two front-end channels (which include a double-range CSA with a real-time network for feedback control, a CDS filter and an output buffer) and nine channels with fully differential, switched capacitor cyclic ADC, implemented around two alternative differential opamp architectures.

Measurements on the front-end section have demonstrated a dynamic range of 52.6 pC, an ENC of 2280 e⁻/\text{FWHM} at 0 detector capacitance, with a slope of 7.5 e⁻/\text{pF}, a non-linearity below 0.6% over the full dynamic range. The power consumption of a front-end channel is 2.8 mW.

Tests on the ADCs have shown that:
1. 100% of the channels convert correctly and display the expected power consumption (171 ADC channels tested at 100 ksp and 1 Msp). This result indicates that the random device mismatch problem that affected the first version of the ADC has been solved.

2. Full range (1.7 V differential) operation shows that the ADC sensitivity is close to the design one. Linearity is affected by loop gain error due to mismatches in the values of the capacitors defining the multiplication by two. On the basis of the results on this prototype, we have finalized the design of a fully operative “final” ASIC in two versions:

a) CASIS1.2A: “analog” version (without ADC), with 16 front-end channels followed by an analog multiplexer and an output buffer. The ASIC also includes an input calibra-
tion circuit. This design has been already produced within an Europractice [15] prototyping run at the end of 2009 and is currently under test.

b) CASIS1.2B: “complete” 16-channel version with one ADC/channel. To improve linearity, the ADC design has been modified by including both capacitor averaging and digital correction techniques. This has required the use of three differential opamps instead of two, and the use of a three-phase clock. In addition, the single-ended to differential conversion has been modified to keep the input common mode voltage constant. We plan to submit this design for prototyping by September 2010.